Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	(second and memory and data and instruction and current and consumption and tariff and system and computation and electricity and consumed).clm.	US-PGPUB	OR	ON	2005/08/01 14:42
L3	2	((second other subsequent additional) and (register cache memory) and (information data) and instruction and current and (consumption usage) and (tariff tax fee rate) and system and (computation calculation calculating calculate compute calculated computing computed) and (electricity energy) and (consumed used)).clm.	US-PGPUB	OR	ON	2005/08/01 14:45
L4	6	(first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)). clm.	US-PGPUB	OR	ON	2005/08/01 14:49

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	diewald-horst.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/01 14:55
L2	11	diewald-h.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/01 14:55
L3	76	diewald.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/01 14:55

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	447	702/45.ccls.	US-PGPUB; USPAT	OR	OFF	2005/08/01 14:59
L3	620.	702/189.ccls.	US-PGPUB; USPAT	OR	OFF	2005/08/01 14:59

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	447	702/45.ccls.	US-PGPUB; USPAT	OR	OFF	2005/08/01 14:59
L3	620	702/189.ccls.	US-PGPUB; USPAT	OR	OFF	2005/08/01 14:59
L6	1	(l2 l3) and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)) and (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR	OR	ON	2005/08/01 15:04
L8	147	(first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)) and (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR	OR	ON	2005/08/01 15:08